REMARKS/ARGUMENTS

Claims 11-30 remain pending.

As the claims are not amended here, for reference, Claim 11 is:

> 11. A process for obtaining a thin layer made of a first material on a substrate made of a second material called a final substrate, the process comprising, in the order as hereinafter set forth:
>
> bonding a thick layer of a first material by one of its main faces on the final substrate at an interface followed by implanting gaseous species in the thick layer of the first material to create a weakened zone delimiting said thin layer between the interface and the weakened zone, or implanting gaseous species in a thick layer of a first material to create a weakened zone followed by bonding said thick layer of said first material by one of its main faces on the final substrate at an interface thereby delimiting said thin layer between the interface and the weakened zone;
>
> depositing a layer of a third material to form a self-supporting layer on a free face of the thick layer made of the first material; and
>
> fracturing the structure comprising the final substrate, the thick layer of the first material and the layer of the third material at the weakened zone to supply the substrate supporting said thin layer.

The rejection under 35 USC 102(e) citing to U.S. 7,115,481 to Ghyselen is not applicable because (A) the date upon which the Ghyselen patent is available under 102(e) is October 14, 2003 whereas the present application claims the benefit of FR 03 50207 filed June 6, 2003 and (B) contrary to the conclusion set forth in the Action Ghyselen does not describe "depositing a layer of a third material to form a self-supporting layer. . ." as in claim 11 because Ghyselen describes a stiffening substrate. Further details on point (B) are provided below.

While the Examiner concluded that the method Applicants claim requires a self-supporting layer, the Examiner appears not to have recognized that the "stiffening substrate" in the method Applicants claim is quite different from the "self-supporting layer" described by Ghyselen in col. 6. While Applicants understand that, during the prosecution of an

application in the Office, claims are to be given their broadest reasonable interpretation consistent with the teaching in the specification (*In re Bond*, 710 F.2d 831, 833 (Fed. Cir. 1990)), it is error to disregard express limitations in the claims. The Examiner may not set up a "strawman" claim and reject it rather than subject matter encompassed by the actual claims.

The plain language of Applicants' claims requires "depositing a layer of a third material to form a self-supporting layer" (cf Claim 11). It is known in the are that a stiffening substrate is not a self-supporting layer (see attached publication of Ackermann et al (2003) *Appl Surf Sci* 212-213:411-416, note the title). Contrary to a substrate which is rigid because of its thickness, a self-supporting layer is a layer of a material having a thickness just sufficient for its use.

As described on page 2, lines 3-6 of the present application, it is known to use a process to obtain very thin layers, (typically less than 0.1 μm) However, problems can arise when trying to obtain very thin layers (typically less than 0.1 μm) due to the appearance of defects, for example blisters, starting from the bonding interface. The present application shows, as an example, the thickness of 4 μm for a self-supporting layer of silicon oxide (page 8, lines 10-13 and page 11, lines 3-7). The diagram of FIG. 3 in the present application and the text at page 12, line 9 to page 13, line 3 permits one to determine the relation between the minimum thickness of the self-supporting layer with respect to the temperature of fracture.

More specifically that portion of the specification, FIG. 3 is a diagram in which the ordinate represents the thickness e of the SiO_2 deposit and the abscissa represents the annealing temperature T. The curve shown in this diagram delimits the area in which the self-supported silicon layer is transferred (the area located above the curve) from the area in which a "blister" occurs on the silicon layer (the zone located below the curve).

This diagram shows that the temperature of separation (or fracture) with transfer of a self-supported dual layer does depend on the deposited oxide thickness. The temperature is

higher if the oxide is thinner. Consequently, the thickness of the fractured silicon layer needs to be added to this oxide thickness. Therefore, in particular it is possible to deduce the minimum thickness of oxide layer necessary for the fracture to be induced at a certain temperature. Therefore, it can be seen that the "threshold" fracture thickness at 600°C. is exceeded for 4 .μm of deposited oxide. Therefore, it is possible to control the thinning procedure by controlling the thickness of the deposited self-supporting layer, thus preventing "blistering" and exfoliation phenomena that would occur if the deposited layer is thinner than the "threshold" thickness.

Applicants submit that the Examiner erred in broadly interpreting the scope and content of the subject matter claimed in a manner inconsistent with the plain language of the claims and the teaching of the Specification.

Withdrawal of the rejection is requested.

A Notice of Allowance is also requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Daniel J. Pereira, Ph.D.
Attorney of Record
Registration No. 45,518

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/07)

Available online at www.sciencedirect.com

SCIENCE @ DIRECT®

Applied Surface Science 212–213 (2003) 411–416

applied surface science

www.elsevier.com/locate/apsusc

Micro-patterning of self-supporting layers with conducting polymer wires for 3D-chip interconnection applications

J. Ackermann[a,*], C. Videlot[a], T.N. Nguyen[b], L. Wang[b], P.M. Sarro[b], D. Crawley[c], K. Nikolić[c], M. Forshaw[c]

[a]*Laboratoire des Matériaux Moléculaires et des Biomatériaux, Faculté des Sciences de Luminy/CNRS UMR 6114–Case 901, 163 avenue de Luminy, F-13288 Marseille Cedex 09, France*

[b]*Technische Universteit Delft, DIMES-ECTM, P.O. Box 5053, 2600 Delft, The Netherlands*

[c]*Department of Physics and Astronomy, University College London, Gower Street, London WC1E 6BT, UK*

Abstract

Highly conducting polymers have attracted much interest because of their potential applications in sensors and electronic devices. By the use of templates like porous membranes during polymerization conducting molecular wires can be formed with highly anisotropic properties which can be used as interconnecting layers in a three-dimensional (3D)-chip stacking. We focussed on two electrochemical polymerization (ECP) techniques to produce molecular wires based on polypyrrole (PPy) embedded in isolating porous polycarbonate membranes as self-supporting layers. The growth of the polymer through the membrane pores was investigated in order to achieve a good conductivity through the pores, but with a small cross-talk between them. A new polymerization technique based on a structured cathode has been developed in order to control the polymerization locally. By that technique micro-patterned membranes with separated conducting polymer wires could be produced.

PACS: 72.80.Le; 84.32.D; 81.16.Dn; 85.40.Hp

Keywords: Polymers; Molecular interconnections; Self-assembly; Patterning

1. Introduction

The development of classical semiconductor IC technology is driven by a constant reduction in structure size, however the limited possibilities of miniaturisation might lead to problems in the future. One challenging option to overcome this dead end is to take into account the third dimension in the chip design leading to new concepts of three-dimensional (3D)-chip stacking and even new chip designs itself.

The long-term objective of the European CORTEX project (hybrid molecular/electronic retina–cortex structure) is to develop a new technology for three-dimensional computer structures [1]. For this, the feasibility of very high-density, three-dimensional molecular wires between electrical contacts on separate, closely, spaced, semiconductor chips had to be demonstrated. These could contain any combination of microelectronic, nano-electronic and molecular computing devices. An example of such a structure is a fault-tolerant, 3D, retina–cortex computer. The

* Corresponding author. Tel.: +33-4-91-82-95-88; fax: +33-4-91-82-95-82.
E-mail address: ackermann@luminy.univ-mrs.fr (J. Ackermann).

0169-4332/03/$ – see front matter © 2003 Elsevier Science B.V. All rights reserved.
doi:10.1016/S0169-4332(03)00418-5

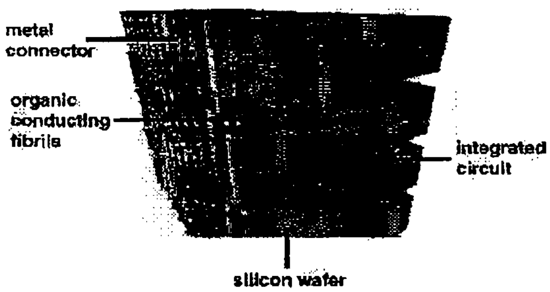


Fig. 1. Cortex 3D-chip stacking with chip interconnections accomplished by organic conducting fibrils.

investigation of such structures is believed to be important, since there are considerable questions about the technological feasibility of two-dimensional computing structures at the nano-scale.

In this context, we were investigating the development of polymer-based micro- and nano-wires in self-supporting insulating layers, which could be used as a chip interconnecting matrix (Fig. 1).

Conducting polymers have attracted much interest in the polymer field due to their electrical conductivity and their potential application in biosensors, conductive paints, batteries, modified electrode and electronic devices [2,3]. The conductive polymer material used is polypyrrole (PPy) [4–6]. It is highly stable in air, intensely black coloured in its doped form (conducting form) and transparent green when undoped. The polymer can be fabricated both by chemical and electrochemical polymerization (ECP) in several solvents like acetonitrile or water. In this present work, the conducting polypyrrole-based wires were used to transfer electrical signals from one surface of the isolating support layer to the other surface. Where in a previous work we focused mainly on polymer wires produced by chemical polymerization in a porous membrane [7] here the synthesis of the polypyrrole was realised by a electrochemical polymerization process. By using an ECP process with homogenous electrodes, the growth of the polymer through the membrane pores was found to be non-uniform over a large area. An analyse of the membrane surface shows polymer wires sticking out of the membrane with partly being interconnected while other pores were still not yet filled completely. In order to control the polymer growth, a modified ECP process was developed which allows an external control of the polymer growth to avoid any wire interconnections over the surface and to have a maximal signal transport through the membrane. By using a structured cathode, which consists of conducting metal pads surrounded by isolating areas, a controlled local growth of the polymer starting from the metallic pads on the cathode can be established. The so called directional electrochemical polymerization (DEP) technique turned out to be a powerful method to pattern the self-supporting layers, i.e. porous membranes, with conducting polymers. We could demonstrate a micro-patterning of a porous membrane with conducting polymer wires of diameters between 300 and 100 μm.

2. Experiments

The monomer pyrrole is a commercial product (Aldrich, 98%) and was purified by distillation prior to use. As self-supporting layer polycarbonate commercial filtration membranes with different pore diameters were used. The polycarbonate membrane, delivered from Millipore and Whathman, were 10 μm thick and had pore diameters ranging from 30 to 1000 nm. The pore density of these membranes was checked with a scanning electron microscope and found to be between 6 and 9%. The 100 nm pore size Wathman membranes were produced by track-etching which guaranties a negligible amount of interconnections between the pores due to a directional fabrication process. Thus, possible cross-talk of the polymer nano-wire inside the membrane could be avoided. The main part of our study presented here was realised on the 100 nm pore size Wathman membranes. The synthesis of the polypyrrole to form the conducting wires was realised by electrochemical polymerization with homogenous electrodes. A metallic layer was first evaporated onto one side of the membrane with a thickness greater than the pore size to close the pores and to serve as an electrode in the ECP process. The membrane was then mounted on the cell so that the Au side was in contact with the flat cathode formed by a highly doped Si wafer (Fig. 2a). In the directional electrochemical polymerization (DEP) process instead of the homogenous cathode a specially designed patterned electrode was used (Fig. 2b).

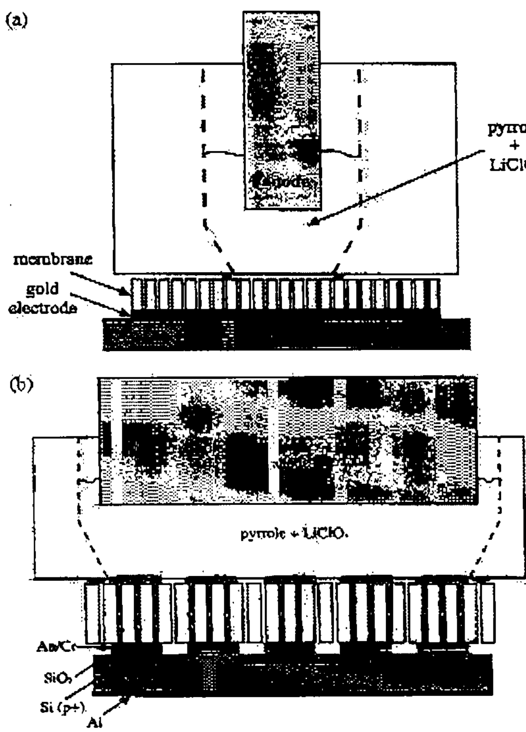


Fig. 2. Scheme of the electrochemical polymerization (ECP) process (a) and the directional electrochemical polymerization (DEP) process (b).

The patterned cathode was formed by structured highly p-doped Si wafer with top metal island (Au/Cr, 300 nm thick) isolated by surrounding SiO_2. The pads had a surface of 100 μm × 100 μm or 300 μm × 300 μm and a height of 5 μm with respect to the SiO_2 surface. A metallic layer (Al) was deposited on the back side of the cathode to ensure a good contact with a metallic plate contact of the polymerization cell. The membrane was first rinsed in ethanol and directly mounted onto the structured cathode. The ethanol was used to make the membrane more elastic and improve the contact of the membrane and the cathode. In both processes, the polymerization was performed at room temperature in a one-compartment cell with a homogenous Pt counter electrode and an Ag/AgCl reference electrode. The solution contained 0.1 M pyrrole with 0.1 M $LiClO_4$ as electrolyte. The polymer was grown potentiostatically at 1.2 V using an EG&G Princeton Research Model 173 potentiostat/galvanostat. A short pulse of a higher voltage (2.5 V) during the first 10 s of the polymerization was applied in order to produce a homogenous growth of the polymer on the cathode pads. After polymerization, the polymer-filled layers were rinsed for 2 min in deionised water and ethanol, respectively. The conductivity and cross-talk measurements were carried out with a specially designed test rig [7] combined with a Hewlett-Packard 4140B pico-amperemeter-dc voltage source. In the case of ECP-processed membranes, the Si upper chips were patterned with metal pads (300 nm Cu or Au/Cr layer) with a surface of 100 μm × 100 μm or 300 μm × 300 μm and a height of 5 μm in order to exercise a high pressure locally on the self-supporting layer. The Au film on the back side of the membrane was removed prior to the cross-talk measurements. For the characterisation of DEP-processed membranes uniform contact upper chips were used. SEM micrographs were done with a JEOL Field Emission Gun Scanning Electron Microscope (FEG-SEM, model JSM 6320F) at 5 kV. To enhance the contrast a 40 Å layer of Au was evaporated on top of the membrane surface.

3. Conductivity measurements

The conducting polymer containing self-supporting layers were positioned between upper and bottom chip of the test rig [7] and by using two-probe measurement the resistance of the isolating layers pattern with the conducting polymer was determined from I–V curves.

The conductivities $\sigma_\perp$ and $\sigma_\parallel$ were calculated from:

$$R = {\sigma_{\perp,\parallel}}^{-1} \frac{l}{A} \quad (1)$$

with l being the thickness of the self-supporting layer for $\sigma_\perp$ and the distance between the two pads for $\sigma_\parallel$; A the surface of the contact pads.

The measurement of $\sigma_\parallel$ was done by using an isolating upper chip in the set up. In this configuration, the current transport between two contact pads on the bottom chip can go only via interconnected conducting fibrils inside the self-supporting layer or via polymer depositions on the surface of the layer and thus the cross-talk could be measured.

As cross-talk ratio we defined:

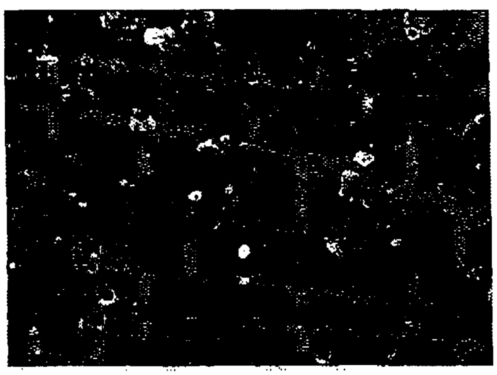
$$CT = \frac{\sigma_\perp}{\sigma_\parallel} \quad (2)$$

The development of a process to produce a polymer-filled self-supporting layer with a high CT value combined with a high conductivity through the membrane ($\sigma_\perp$) were the objective of our study.

4. Polymer nano-wires filled porous membranes

During the ECP process, the amount of the grown polymers inside of the membrane is given by the polymerization time at a certain voltage (1.2 V). In order to avoid cross-talk between the polymer wires, the polymerization has to be stopped prior to the formation of wire interconnections on the surface and thus the creation of cross-talks. Fig. 3a and b show two surfaces of ECP-processed membranes with different polymerization times. For a short polymerization process (Fig. 3a) the polymer nano-wires just grown out of the membrane pores form a mushroom shape (no. 4) which should be favourable to contact the wires by external contact pads. However, a lot of pores not yet or just partly filled (nos. 1–3) can be found on the same membrane revealing a strongly non-uniform growth process. In order to fill all the pores, a longer process time was applied which leads to a modified surface covering shown in Fig. 3b. Here a large amount of polymer wires interconnected over the surface are observed which gave rise to a high amount of cross-talk between wires. In conclusion, it can be established that the polymer growth through a porous membrane is strongly non-uniform over a large area and thus very difficult to control in order to form well-separated molecular wires. Therefore, by using the standard ECP process, a compromise has to be taken between conductivity and cross-talk ratio. The best result produced by ECP was polymer wires embedded in a membrane with a conductivity of 0.14 S/cm and a cross-talk ratio of 46. In order to improve the electric properties of the membrane, post-treatments on the ECP-processed membrane has to be performed as it was discussed in the previous work [7]. However, a real control of the polymer formation could open a much better performance of such a polymer matrix. Therefore, a modified electrochemical polymerization process called DEP was developed and is discussed in the following paragraph.

(a)



(b)

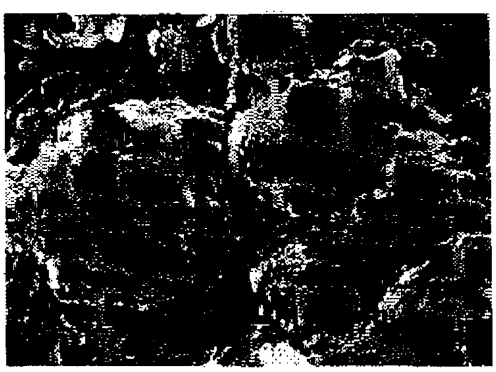


Fig. 3. SEM pictures of the surface of polymerised membranes (Whathman, 100 nm pore size) obtained by a ECP process with different process time: (a) $T_{poly} = 2$ min; (b) $T_{poly} = 4$ min.

5. Micro-patterning of porous membranes with a DEP process

In general, the formation of a polymer by a ECP process takes place at a conducting cathode where the monomer is oxidised and a successive polymer chain is formed. Therefore, a current has to flow from the monomer to the cathode. A DEP process was based on the use of a structured cathode consisting of metallic pads surrounded by isolating SiO_2 areas. During polymerization the polymer formation was limited to the areas of conducting metallic pads on the cathode. By placing a porous membrane in very closed

(a)

(b)

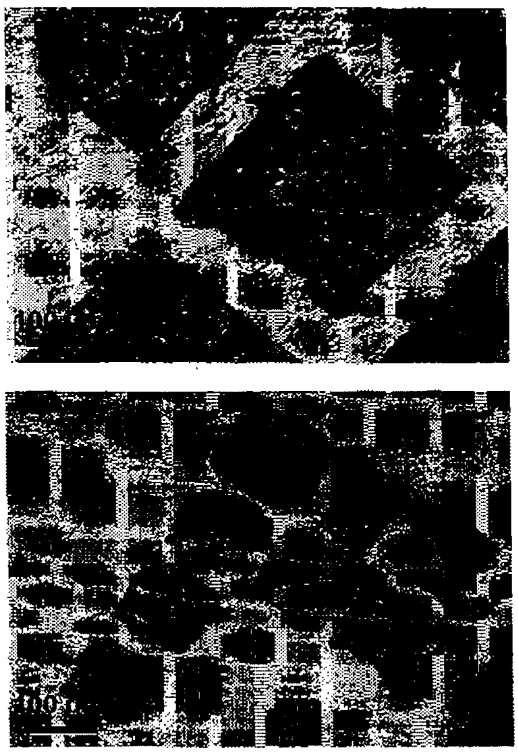


Fig. 4. Optical images of polymerised membranes (Whathman, 100 nm pore size) obtained by a DEP process with cathode pads of 300 μm × 300 μm (a) and 100 μm × 100 μm (b).

contact with the structured cathode during a DEP process, the structure of the metallic pads were imprinted on the membrane by polymer wires grown locally through it. By that technique, a micro-patterning of the membrane with polymer wires was performed depending on the metallic pattern produced on the cathode before. In Fig. 4a, a membrane containing polymer pattern of 300 μm × 300 μm each pad is shown. The polymer pads were separated with highly isolating areas between them, i.e. the pure polycarbonate membrane, and finally there were no cross talk between the polymer micro-wires. Additionally, the polymer pads could be grown in that way that they stuck several micrometer out of the membrane without an appearance of cross-talk which reduced the pressure needed to receive a good contact to the polymer wires in the test rig.

For smaller structures of 100 μm × 100 μm and a distance of 30 μm between them (Fig. 4b) a enlargement of the micro-pattern imprinted on the membrane was observed. This might be due to the fact that the distance between the metal pads of 30 μm and the height of a pad of 5 μm were in the same order which lead to a high leakage current under the membrane and thereby to a formation of the polymer beside the pads. However, this problem should be solved by the use of hidden metal pads inside the SiO_2 layer, which will be part of the next cathode generation of structured pads. The conductivity of the patterned membranes was 0.5 and 0.3 S/cm for a pad size of 300 and 100 μm, respectively, which are improved values compared to a standard ECP process with a guaranty of no cross-talk between the polymer micro-wires.

6. Conclusion

The study of the polymer growth through porous membrane by standard ECP and a modified DEP process gave interesting results towards a deeper understanding of the possibilities and limits for the design of conducting molecular wires in self-supporting layers as interconnections in future 3D-chip stacking technologies. With the ECP process we could demonstrate a high conductivity of 0.14 S/cm in combination with a cross-talk ratio of 46. The DEP process which had a structured cathode turned out to be a powerful technique to perform a micro-patterning of the membrane with polymer wires. The DEP-processed polymer micro-wires demonstrated a conductivity of 0.5 S/cm, but without any cross-talk which is very important for a perfect signal transfer in the 3D-chip stacking.

Acknowledgements

This work was supported by the European Commission in form of the European CORTEX project called "Design and Construction of Elements of a Hybrid Molecular/Electronic Retina-Cortex Structure" no IST-CT1999-10236. We are especially grateful to C. Rebout for his helpful technical assistance, LMMB, Marseille, France. We are also grateful to Ing. S. Nitsche from the CRMC2 of Faculté des Sciences

de Luminy in Marseille, France, for SEM pictures of the membranes.

References

[1] New Scientist, 7 October (2000) 41.
[2] G. Zotti, Synth. Met. 51 (1992) 373.
[3] S. Holdcroft, Adv. Mater. 13 (2001) 1753.
[4] R.H. Friend, Conductive polymers. II. From science to applications, Rapra review Reports, vol. 6, no. 3, report 63, Rapra, 1993.
[5] J. Duchet, R. Legras, S. Demoustier-Champagne, Synth. Met. 98 (1998) 113.
[6] E. Ando, S. Onodera, M. Lino, O. Ito, Carbon 39 (2001) 101.
[7] J. Ackermann, D. Crawley, M. Forshaw, K. Nikolic, C. Videlot, Surf. Sci., in press.